

REMARKS

Reconsideration of the present application is respectfully requested.

The Examiner's thorough examination of the present application is commended.

The rejection of claim 1 under 35 USC 102(e) as being anticipated by Bowes et al. is respectfully traversed.

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist and Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983); *SSIH Equip. S.A. v. USITC*, 718 F.2d 365, 218 USPQ 678 (Fed. Cir. 1983). Stated another way, for a prior art reference to anticipate in terms of 35 U.S.C. 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990) (emphasis added.).

Claim 1 features retrieving a first portion of the recorded data via the bus and updating some of the registers via the bus. The Office Action contends that the claimed bus is disclosed by bus 214 (and bus 262, see below) of Bowes et al. The Office Action also contends that elements 312, 324 of Bowes et al. disclose the claimed registers. However, that is not enough to support this rejection. In particular, Bowes et al. nowhere expressly disclose updating some of the registers via the bus.

The Office Action recognizes this lack of express disclosure by Bowes et al. in the comment under the Response to Arguments section in the present Office Action. Stated there is "Bowes physically does not show an connection between the data bus 262 or the I/O bus 214 and registers 314 and 324 but is inherently the I/O bus having an connection to connect registers 314 and 324 in order to update the count registers 314 and 324 after data is transferred from the I/O controller to the FIFO via the I/O bus 214 (see column 14 lines 44-51)." From this quote the Office Action is relying on inherency to show that Bowes et al. disclose updating some of the registers via the bus. This reliance is incorrect.

Bowes et al. disclose that elements 314 and 324 are updated by decrementing 2 from the address by adder 380. Adder 380 is controlled by a signal on lead 376 that is generated from a RdDecBy2 signal and a WrDecBy2 signal. Those signals are provided by block 330 and block 320, respectively. None of the signals input to those blocks are disclosed in Bowes et al. as

being part of buses 214 or 262. The Office Action's contention that buses 214 and 262 are connected to elements 314 and 324 is not supported in Bowes et al. Therefore, Bowes et al. do not identically show retrieving a first portion of the recorded data via the bus and updating some of the registers via the bus as featured in claim 1. As such, claim 1 is not anticipated and is allowable over Bowes et al.

The rejection of claims 2-5 under 35 USC 103(a) as being unpatentable over Bowes et al. in view of Glover is respectfully traversed.

Claims 2-5 depend from claim 1. Claim 1 is not taught or suggested by Bowes et al. Glover does not overcome this deficiency of Bowes et al. Therefore, claims 2-5 are not obvious and are allowable due to their dependence on allowable claim 1.

The rejection of claims 6, 8, 9, 11-14 under 35 USC 103(a) as being unpatentable over Bowes et al. and Glover and in view of Nishida is respectfully traversed.

Claim 6 features updating at least some of the read channel register values. The Office Action now contends that registers 366, 316 and 326 are the read channel registers. This is incorrect. Registers 366, 316 and 326 are used by the DMA channel depicted in Fig. 3. However, the DMA channel is not the same as a read channel. Again, see Glover for further details.

In addition, "the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997). In the present case, the specification does not describe a read channel to include a DMA. Therefore, the Office Action is not applying a reasonable meaning to the term read channel as would be understood by one skilled in the art.

In light of all that, registers 316, 326 and 366 are not read channel registers. As a result, Bowes et al. do not teach read channel register values and that reference does not suggest that. Furthermore, the Office Action does not disclose where in the other applied references, Glover and Nishida, this claim 6 feature is taught or suggested. Therefore, claim 6 is not obvious over these three references and is allowable. In addition, claims 8, 9, 11-14 depend from claim 6. Since claim 6 is allowable, these claims are also allowable.

The rejection of claim 7 under 35 USC 103(a) as being unpatentable over Bowes et al., Glover and Nishida, and in further view of Asakawa et al. is respectfully traversed. As explained for claim 6, Bowes et al. are deficient in disclosing the feature of updating at least some of the read channel register values. None of the other three references used in this rejection have been cited to overcome this deficiency of Bowes et al. Therefore, claim 7 is allowable due to its dependence on allowable claim 6.

The rejection of claim 15 under 35 USC 103(a) as being unpatentable over Bowes et al. in further view of Donnan is respectfully traversed. Claim 15 features a memory containing several values indexed by zone identifiers. The Office Action correctly points out that Bowes et al. do not identically show this feature. The Office Action relies on Donnan to show this feature by referring to Donnan's Abstract.

Regardless of what Bowes et al. and Donnan teach or suggest, the combination of these two references is not supported. First, Donnan is not analogous art to the present invention. "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). Donnan is directed to a "method of managing concurrent accesses by a plurality of users to a memory, for reading or writing data in memory zones of the memory on the basis of an index whose value identifies a memory zone in the memory..." (see the Abstract). On the other hand, one field of endeavor can be gleaned from the Summary of the Invention section of the present application: Methods and devices of the present invention update operating parameters and/or read channel registers with a lesser burden on the disc drive's primary processor. Clearly these field of endeavors are quite different.

One problem that the invention is concerned with is updating operating parameters and/or read channel registers with a lesser burden on the disc drive's primary processor. Donnan sets out at col. 2, lines 13-16, that the "object of the invention is to minimize the size of said critical section so as to avoid the phenomenon of users waiting for access to the memory being blocked in the context of a single-processor architecture." This particular problem disclosed by Donnan is not pertinent to the problem cited above for the present invention. Accordingly, Donnan is not analogous art. As such, it is an improper reference that cannot be used in combination with

Bowes et al. Therefore, a prima facie case of obviousness has not been made, which causes claim 15 not to be obvious, but to be allowable.

Even if Donnan is analogous art, there is no teaching, suggestion or motivation from the references, alone or in combination, to combine them. First, nowhere do Bowes et al. teach the need for a memory containing several values indexed by zone identifiers. Furthermore, the purpose of the registers relied on by the Office Action does not suggest the need for that.

Donnan is also similarly deficient in any teach, suggestion or motivation to combine these references. First, contrary to the Office Action's statement, Donnan teach nothing about disc drives. Second, there is no suggestion in Donnan to use its disclosed invention in a DMA controller such as disclosed by Bowes et al. Third, the Office Action provides no objective evidence that knowledge of one skilled in the art combined with these two references would motive one skilled in the art to combine these references. Hence, there is no teaching, suggestion or motivation to combine these references.

Even if those references can be combined, the combination does not teach or suggest the claim 15 feature of the bus controllable by the DMA controller to read from the memory and to update several registers in response to a zone transition event. Claim 15 cannot then be considered obvious in view of this deficiency.

In summary, claim 15 is not obvious and is allowable because Donnan is not analogous art; there is no teaching, suggestion or motivation to combine Bowes et al. and Donnan; and a feature of claim 15 is not taught or suggested even if the references were combined.

The right to agree to or dispute any contention by the Office Actions that were not addressed in any response or amendment shall not be construed as waiving the right to dispute or agree to any such contention. Nor does the absence of disputing or agreeing to the claim preambles being considered as limitations mean that the right to dispute or agree to that is waived.

As explained above, all the pending claims are patentable over the applied references.
The examiner is respectfully requested to allow all the pending claims and new claims 16-20,
and pass this case to issuance.

Respectfully submitted,

SEAGATE TECHNOLOGY LLC
(Assignee of Entire Interest)

Date

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